HUANG, Xinyang

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Education

- **Hong Kong University of Science and Technology** — Hong Kong, China
  Doctor of Philosophy - Computer Science Engineering — *Aug. 2023 - Present*
- **Hong Kong University of Science and Technology** — Hong Kong, China
  Master of Philosophy - Computer Science Engineering; GPA: 3.73/4.0 — *Sept. 2021 - Aug. 2023*
  Courses: *Advanced Algorithms (A-), Computer Network (A-), Machine Learning (A-), Advanced Computer Architecture (A+)*
- **University of Electronic Science and Technology of China** — Chengdu, China
  Bachelor of Science in Network Engineering; GPA: 3.88/4.0 — *Sept. 2017 - June 2021*
  Courses: *Graphic Theory, Stochastic Process, TCP/IP Protocol, Access Network, Signal and System, Digital Circuits, etc.*

Skills Summary

- **Languages**: C/C++, Verilog, Python, MATLAB, JAVA, CUDA, etc.
- **SDK/Library**: DPDK, eBPF/XDP, DOCA, NCCL, RDMA Core, etc.
- **Framework**: BlueField, Corundum, PyTorch, FATE, Spark, etc.
- **Tools**: Vivado/Vitis, Docker, cocotb, MAAS, Keil, etc.

Selected Publications

- **eddos: Efficient, Lightweight, and Elastic Dataplane OS for Data Processing Units**: 1st author, under review
- **Tuning Host Datapath Performance with PipeTune**: 1st author, under review
- **CEIO: A Cache-Efficient Network I/O Architecture for NIC-CPU Data Paths**: co-1st author, SIGCOMM'25
- **Cache-Aware Rate Control for RDMA I/O Congestion**: 2nd author, APNet'25
- **Enabling Efficient GPU Communication over Multiple NICs with FuseLink**: 4th author, OSDI'25
- **Accelerating Privacy-Preserving Machine Learning with GeniBatch**: 1st author, EuroSys'24

Selective Research Experience

- **Optimizations Towards 100Gbps+ Host Networks** — HKUST, Hong Kong
  Researcher, Supervisor: Professor Kai CHEN — *Sept. 2023 - Present*
  - **Tech**: DPDK, DOCA, BlueField, RDMA core.
  - **PipeTune**: Develop an efficient and programmable tuning framework for 100Gbps+ CPU-NIC datapaths
    - **Results and Progress**: Our framework improves the throughput and reduces P99.9 latency of target datapaths (i.e., eRPC, Open vSwitch, etc.) by up to 2.1× and 4.6×, respectively.
  - **CEIO**: Design a cache-efficient I/O architecture based on the latest NVIDIA BlueField 3 DPUs, introducing proactive, credit-based I/O rate control and elastic buffering to eliminate LLC misses in I/O datapaths.
    - **Results and Progress**: CEIO outperforms SOTA solutions by up to 2.9× in throughput and 1.9× in latency. CEIO has been accepted by SIGCOMM'25 (co-1st author).
- **High-Performance and Flexible DPU Infrastructure** — HKUST, Hong Kong
  Researcher, Supervisor: Professor Kai CHEN — *Nov. 2022 - Present*
  - **Tech**: DPDK, BlueField, DOCA, eBPF/XDP, Corundum, Vivado/Vitis, cocotb, Verilog.
  - **eddos**: Extend existing DPU dataplane operating systems (i.e. NVIDIA DOCA) with efficient data movement, lightweight queue management, and elastic context switching.
    - **Results and Progress**: Complete eddos development with 20000+ LoC. Compared to DOCA, eddos improves various DPU workloads (e.g., NF chain, distributed protocols, RDMA, etc.) by up to 4.8× in throughput.
  - **SingNIC**: Design a 100Gbps programmable NIC architecture with on-path MIPS cores.
    - **Results and Progress**: Build an FPGA prototype that can offload XDP programs with line rate.
- **Accelerating Privacy-Preserving Machine Learning (PPML) with GeniBatch** — HKUST, Hong Kong
  Researcher, Supervisor: Professor Kai CHEN — *Dec. 2021 - Oct. 2022*
  - **Tech**: Docker, FATE, Spark, HDFS, Python, CUDA.
  - Design a batch compiler called GeniBatch that translates a PPML program with Partical Homomorphic Encryption into an efficient program with batch optimization.
  - **Results and Progress**: GeniBatch accelerates end-to-end performance for various cross-silo PPML applications from 1.59x to 22.6x. GeniBatch has been accepted by EuroSys'24 (1st author).

Honors and Awards

- Postgraduate Studentship (PGS) award of HKUST - 2021-2022, 2022-2023, 2023-2024, 2024-2025
- Outstanding Academic Scholarship of UESTC for full 3 academic years - 2017-2018, 2018-2019, 2019-2020
- National Innovation and Entrepreneurship Excellent Project - 2018-2019
- Second prize in National Electronic Design Competition - Aug. 2019